MICROWAVE DUAL TRANSISTOR DELIVERS 100W CW

DAVID C. ANDERSON
POWER HYBRIDS, INC.
1742 CRENSHAW BLVD., TORRANCE, CA. 90501

ABSTRACT

This paper reports the results of a dual transistor employing two separate RF bipolar transistors within one package operating near 1 GHz. Significantly improved performance has been achieved over conventional single transistor devices. The final results yielded greater than 100W CW output power with a collector efficiency above 60%.

INTRODUCTION

One of the more recent advances in high power microwave RF transistors has been the development of the dual transistor. Combining two separate transistors into one .400 square inch package has yielded a significant improvement in bandwidth, efficiency, and junction temperature over a single device with the same number of cells. This paper reports the results of a recently developed dual transistor operating near 1 GHz with significantly new performance parameters of high output power with excellent efficiency and low junction temperature in comparison to single transistor devices.[1,2,3] Performance results are summarized in Table I.

TABLE I
PERFORMANCE SUMMARY OF DUAL TRANSISTOR PH8518

FREQUENCY (MHz)	Pout (W)	Vcc (Vdc)	GAIN (dB)	EFFICIENCY (%)	OPERATION
800-975	85	28	8.5	64	CW

While the advantages of parallel combining microwave transistor cells are well known and useful devices have been in industry use for some time, there comes a limit for combining wherein performance degradation occurs düe to package parasitics, uneven power distribution, poor junction temperation profiles, or uneven impedance matching. A recent UHF solution to the impedance problem has been the development of a dual or "balanced" transistor.[4] This is a four-leaded device employing two separate transistors within one package with a common ground connection.

For microwave operation, the advantages of the dual transistor are greatest in reducing the problems associated with cell combining. Therefore, better power sharing and improved thermal profiles can be expected. Additionally, the dual transistor enables the normally low input and output impedance of the conventional transistor to increase by a factor of two thereby making broadband matching easier since fewer low Q matching sections are needed* (Figure 1).

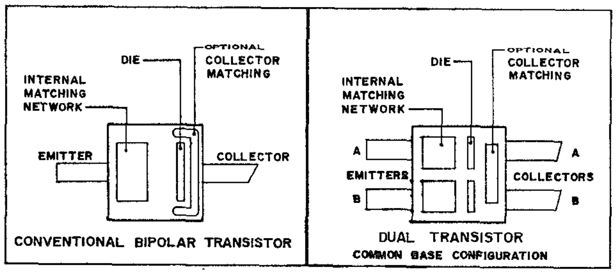

Figure 1 Internal matching schemes for the conventional and dual transistors

The bandwidth benefits of a dual device are really linked to their type of operation rather than the reports that push-pull is superior. Dividing the number of cells of a conventional device by two and creating a dual device does not change the bandwidth capabilities of the original device. This is true since the inherent bandwidth of a device is dependant upon the real part of the output impedance (Rp) and its Cob.[5,6]

$$BW = \frac{K_1}{Rp\ Cob} = \frac{K_1}{2\ R_p\ \frac{Cob}{2}}$$

(Conv. Device) (Dual Device)

However, by operating a dual device in push-pull and by careful selection of the frequency range and operating conditions, it can offer improved bandwidth by reducing the common mode inductance, cancelling out the generation of second harmonics and, most importantly, by offering improved cell power sharing.

THE DEVICE

Internal symmetrical low Q matching was used on the input side of the dual device to achieve a return loss >10 dB. No matching was needed on the collector at the frequency used; however, a significant advantage of the dual device in push-pull operation is the ease of shunt inductor collector matching, whereby a single inductor between the collector pads performs the matching and avoids the need of lossy and bulky MOS bypass capacitors (Figure 2). For high power devices at certain frequencies, such collector matching aids broadband performance while reducing the devices' construction complexity over conventional bipolar transistors.

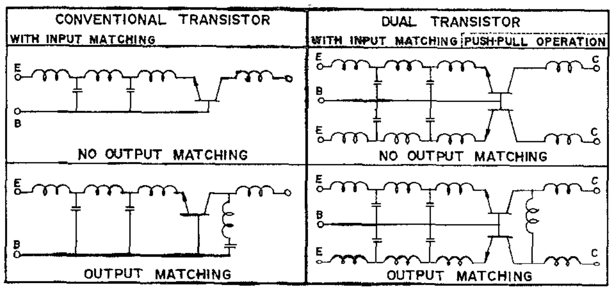

Figure 2 Comparison between the internal matching networks used for the conventional and dual microwave power transistors.

The transistor cells utilize a matrix emitter geometry with laterally diffused ballast resistors and employ gold metalization. Gold is used extensively to maximize reliability by minimizing potential metal migration. Each side of the dual device has 24 cells that are parallel combined and bonded to wide MOS capacitors and input/output leads (Figure 3). The wide leads provide for a uniform current distribution throughout each side of the device thereby achieving greater junction temperature uniformity for the overall device. The entire assembly is made in a stripline hermetic package made of alumina and berylia ceramic.

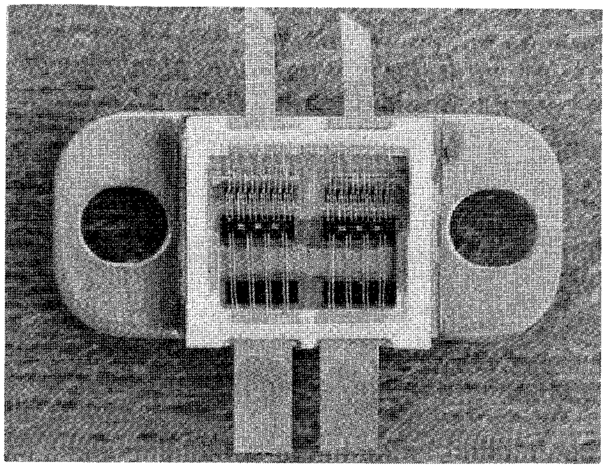

Figure 3 Inside view of packaged transistor showing bonding configuration (Power Hybrids PH 8518).

THE CIRCUIT

Figure 4 shows the actual circuit that was used. Each lead of the dual device was matched to 50 Ω and the tuning was done independently which simplified the tune-up effort. Optimum performance was achieved by operating the device in push-pull operation; however, in phase and quadrature drive worked, but not as well. In push-pull operation the side-to-side interaction is minimized thereby making tuning easier, and additionally, efficiency is improved 10% yielding lower junction temperatures.

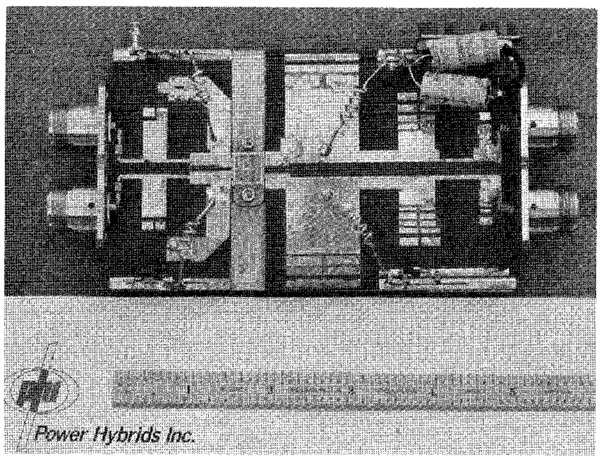

Figure 4 View of the fixture used to match the dual transistors' four ports to 50 Ω (PH 8518).

The push-pull drive source consisted of a 90° quadrature power splitter and an additional 90° phase shifter which resulted in a 180° phase split. This technique was used to provide the lowest source and load VSWR across the frequency range. The splitter and combiner losses were less than 0.2 dB from 800-975 MHz and the maximum VSWR was 1.2:1.

PERFORMANCE

As mentioned, the circuit tune-up was relatively straightforward. Initial design parameters for the circuit topology were obtained from a computer optimization of the devices' impedances. Once tuned and connected to the push-pull drive and load mentioned above, the circuit was checked for current sharing between side A and B. Excellent sharing was observed with maximum current differences of less than 15%. This could be reduced further through improved splitter design since the greatest differences in current sharing occurred at the band edges where the drive power splits were uneven.

Output saturation occured above the 100W CW level with V_{CC} = 28 Vdc, and gain and collector efficiency measurements were >8.5 dB and >60% respectively. At V_{CC} = 32 Vdc, the saturated output power approached 120 W with a flange temperature of 30°C. These high power levels are consistant with current technology at 1 GHz[7] while providing the advantages of the dual transistor design.

Junction temperature measurement showed an excellent thermal distribution with no hot spots (Figure 5).

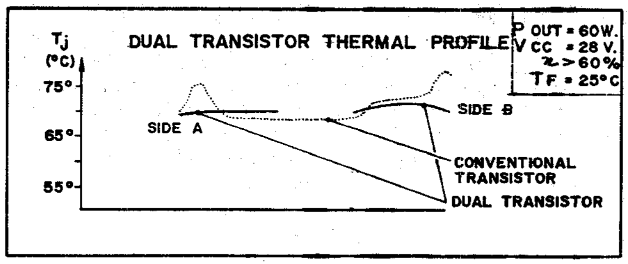

Figure 5 Thermal profile of the dual and conventional transistors on an averaged basis. (Dual device PH 8518).

Transfer performance was measured and no instabilities were observed at any drive level. This typically indicates favorable results would be expected if this device were used in pulse operation for a radar system. Device ruggedness was not thoroughly checked, however a negligible failure rate was observed when these devices were operated in hard saturation (1.1:1 load VSWR).

SPLITTER/COMBINER CONSIDERATIONS

Other types of power splitters yielding 180° phase differences were tried and good performance was achieved, although some of them cause instabilities during drive-up. One of the more practical designs tried was the compensated balun design[8], which could be produced easily because the microstrip concept was employed. A single two-sided PC board was mounted in a hollowed-out heatsink thereby providing three conductive planes to create the transformation from 50 Ω unbalanced to 50 Ω balanced. Figure 6 shows a photograph of the total circuit using this compensated balun concept. The overall circuit topology could be reduced further by using alumina or other high K dielectric material, and the final version of a total circuit with the splitters and combiner incorporated would be only slightly larger than a conventional bipolar fixture.

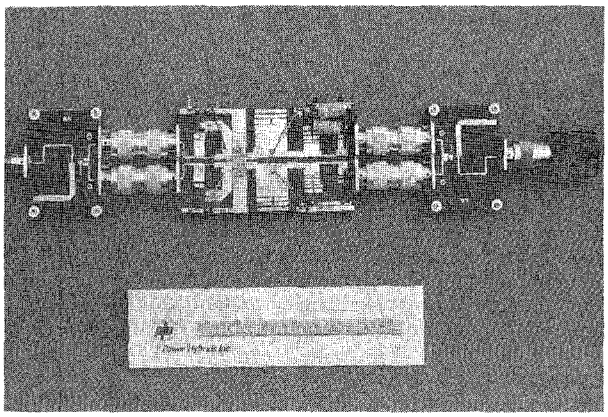

Figure 6 Test fixture utilizing the single PC board compensated balun splitter and combiner.

CONCLUSION

The dual transistor concept together with the push-pull circuit yields excellent output power with improved bandwidth, efficiency and junction temperature over the conventional RF bipolar device. This effort showed that RF transistors employing the dual transistor concept can meet requirements for high power, efficiency, and reliable operation (low T_j) into the microwave range of frequencies. Modern produceable splitters/combiners with good VSWR and low loss are achievable and add minimally to the overall cost while providing a method of successfully using the dual transistor design advantages.

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* Some articles refer to an impedance change of four times which is correct when transformer matching a dual device operated in push-pull operation; however, the basic impedances of each side of the dual device are twice that of the conventional device.